DATA SHEET

74LVCH32374A

32-bit edge-triggered D-type flip-flop with 5 V tolerant inputs/outputs; 3-state

Product specification
Supersedes data of 1999 Nov 24

2004 May 24

Philips
Semiconductors

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32-bit edge-triggered D-type flip-flop with 5 V tolerant inputs/outputs; 3-state

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FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MULTIBYTE flow-trough standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bushold
- Complies with JEDEC standard JESD8-B/JESD36
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +85 °C
- Packaged in plastic fine-pitch ball grid array package.

DESCRIPTION

The 74LVCH32374A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, the outputs can handle 5 V. These features allow the use of these devices in a mixed 3.3 V or 5 V environment.

The 74LVCH32374A is a 32-bit edge-triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. The 74LVCH32374A consists of 4 sections of 8 edge-triggered flip-flops. A clock (pin nCP) input and an output enable input (pin $n\overline{OE}$) are provided per 8-bit section.

The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH nCP transition.

When pin $n\overline{OE}$ is LOW, the contents of the flip-flops are available at the outputs. When pin $n\overline{OE}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of pin $n\overline{OE}$ does not affect the state of the flip-flops.

The 74LVCH32374A bushold data input circuits eliminate the need for external pull-up resistors to hold unused inputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nCP to nQn	C_L = 50 pF; V_{CC} = 3.3 V	3.4	ns
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nQn	C_L = 50 pF; V_{CC} = 3.3 V	3.5	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nQn	C_L = 50 pF; V_{CC} = 3.3 V	3.9	ns
f_{max}	maximum clock frequency	C_L = 50 pF; V_{CC} = 3.3 V	150	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation per flip-flop	V_{CC} = 3.3 V; notes 1 and 2		
		outputs enabled	19	pF
		outputs disabled	12	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	BALLS	PACKAGE	MATERIAL	CODE
74LVCH32374AEC	–40 °C to +85 °C	96	LFBGA96	plastic	SOT536-1

FUNCTION TABLE

See note 1.

OPERATING MODE	INPUT			INTERNAL FLIP-FLOP	OUTPUT
	$n\overline{OE}$	nCP	nDn		nQn
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

Note

1. H = HIGH voltage level;
   h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition;
   L = LOW voltage level;
   l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition;
   Z = high-impedance OFF-state;
   ↑ = LOW-to-HIGH CP transition.

PINNING

BALL	SYMBOL	DESCRIPTION
A1	1Q1	flip-flop output
A2	1Q0	flip-flop output
A3	$1\overline{OE}$	output enable input (active LOW)
A4	1CP	clock input
A5	1D0	data input
A6	1D1	data input
B1	1Q3	flip-flop output
B2	1Q2	flip-flop output
B3	GND	ground (0 V)
B4	GND	ground (0 V)
B5	1D2	data input
B6	1D3	data input
C1	1Q5	flip-flop output
C2	1Q4	flip-flop output
C3	V_{CC}	supply voltage
C4	V_{CC}	supply voltage
C5	1D4	data input
C6	1D5	data input
D1	1Q7	flip-flop output
D2	1Q6	flip-flop output
D3	GND	ground (0 V)
D4	GND	ground (0 V)
D5	1D6	data input
D6	1D7	data input
E1	2Q1	flip-flop output
E2	2Q0	flip-flop output
E3	GND	ground (0 V)
E4	GND	ground (0 V)
E5	2D0	data input
E6	2D1	data input
F1	2Q3	flip-flop output
F2	2Q2	flip-flop output
F3	V_{CC}	supply voltage
F4	V_{CC}	supply voltage
F5	2D2	data input

BALL	SYMBOL	DESCRIPTION
F6	2D3	data input
G1	2Q5	flip-flop output
G2	2Q4	flip-flop output
G3	GND	ground (0 V)
G4	GND	ground (0 V)
G5	2D4	data input
G6	2D5	data input
H1	2Q6	flip-flop output
H2	2Q7	flip-flop output
H3	$2\overline{OE}$	output enable input (active LOW)
H4	2CP	clock input
H5	2D7	data input
H6	2D6	data input
J1	3Q1	flip-flop output
J2	3Q0	flip-flop output
J3	$3\overline{OE}$	output enable input (active LOW)
J4	3CP	clock input
J5	3D0	data input
J6	3D1	data input
K1	3Q3	flip-flop output
K2	3Q2	flip-flop output
K3	GND	ground (0 V)
K4	GND	ground (0 V)
K5	3D2	data input
K6	3D3	data input
L1	3Q5	flip-flop output
L2	3Q4	flip-flop output
L3	V_{CC}	supply voltage
L4	V_{CC}	supply voltage
L5	3D4	data input
L6	3D5	data input

BALL	SYMBOL	DESCRIPTION
M1	3Q7	flip-flop output
M2	3Q6	flip-flop output
M3	GND	ground (0 V)
M4	GND	ground (0 V)
M5	3D6	data input
M6	3D7	data input
N1	4Q1	flip-flop output
N2	4Q0	flip-flop output
N3	GND	ground (0 V)
N4	GND	ground (0 V)
N5	4D0	data input
N6	4D1	data input
P1	4Q3	flip-flop output
P2	4Q2	flip-flop output
P3	V_{CC}	supply voltage
P4	V_{CC}	supply voltage
P5	4D2	data input
P6	4D3	data input
R1	4Q5	flip-flop output
R2	4Q4	flip-flop output
R3	GND	ground (0 V)
R4	GND	ground (0 V)
R5	4D4	data input
R6	4D5	data input
T1	4Q6	data input
T2	4Q7	clock input
T3	$4\overline{OE}$	output enable input (active LOW)
T4	4CP	clock input
T5	4D7	data input
T6	4D6	data input

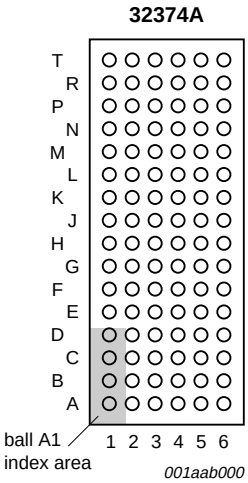


Fig.1 Ball configuration.

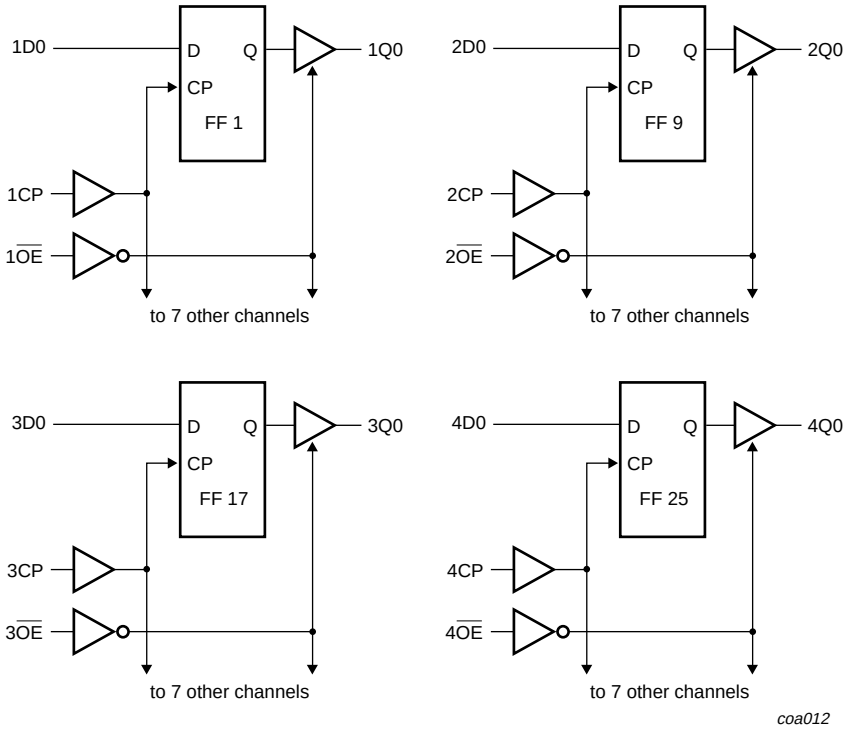


Fig.2 Logic symbol.

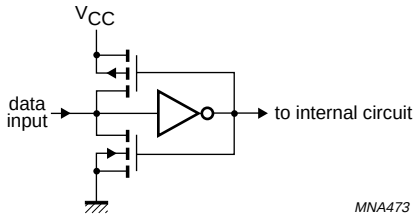


Fig.3 Bushold circuit.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low voltage applications	1.2	3.6	V
V_I	input voltage		0	5.5	V
V_O	output voltage	output HIGH or LOW state	0	V_{CC}	V
		output 3-state	0	5.5	V
T_{amb}	ambient temperature	in free air	–40	+85	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 V to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	V_I < 0 V	–	–50	mA
V_I	input voltage	note 2	–0.5	+6.5	V
I_{OK}	output diode current	V_O > V_{CC} or V_O < 0 V	–	±50	mA
V_O	output voltage	output HIGH or LOW state; note 2	–0.5	V_{CC} + 0.5	V
		output 3-state; note 2	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 V to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current	note 1	–	±200	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +85 °C; note 3	–	1000	mW

Notes

1. All supply and ground pins connected externally to one voltage source.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. Above 70 °C the value of P_{tot} derates linearly with 1.8 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 μA	2.7 to 3.6	V_{CC} − 0.2	V_{CC}	–	V
		I_O = −12 mA	2.7	V_{CC} − 0.5	–	–	V
		I_O = −18 mA	3.0	V_{CC} − 0.6	–	–	V
		I_O = −24 mA	3.0	V_{CC} − 0.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA	2.7 to 3.6	–	GND	0.20	V
		I_O = 12 mA	2.7	–	–	0.40	V
		I_O = 24 mA	3.0	–	–	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; note 2	3.6	–	±0.1	±5	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND; note 2	3.6	–	±0.1	±5	μA
I_{off}	power-off leakage supply current	V_I or V_O = 5.5 V	0.0	–	±0.1	±10	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	3.6	–	0.1	40	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} − 0.6 V; I_O = 0 A	2.7 to 3.6	–	5	500	μA
I_{BHL}	bushold LOW sustaining current	V_I = 0.8 V; notes 3 and 4	3.0	75	–	–	μA
I_{BHH}	bushold HIGH sustaining current	V_I = 2.0 V; notes 3 and 4	3.0	−75	–	–	μA
I_{BHLO}	bushold LOW overdrive current	notes 3 and 5	3.6	500	–	–	μA
I_{BHHO}	bushold HIGH overdrive current	notes 3 and 5	3.6	−500	–	–	μA

Notes

1. All typical values are measured at T_{amb} = 25 °C.
2. For bushold parts, the bushold circuit is switched off when V_I > V_{CC} allowing 5.5 V on the input pin.
3. For data inputs only, control inputs do not have a bushold circuit.
4. The specified sustaining current at the data inputs holds the input below the specified V_I level.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.

AC CHARACTERISTICS

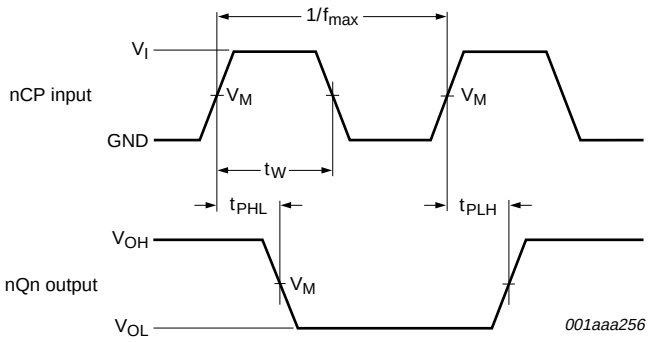
GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\ \Omega$.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C; note1							
t_{PHL}/t_{PLH}	propagation delay nCP to nQn	see Figs. 4 and 7	1.2	–	14	–	ns
			2.7	1.5	–	6.0	ns
			3.0 to 3.6	1.5	3.4(2)	5.4	ns
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nQn	see Figs. 6 and 7	1.2	–	20	–	ns
			2.7	1.5	–	6.0	ns
			3.0 to 3.6	1.0	3.5(2)	5.2	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nQn	see Figs. 6 and 7	1.2	–	12	–	ns
			2.7	1.5	–	5.1	ns
			3.0 to 3.6	1.5	3.9(2)	4.9	ns
t_W	nCP pulse width HIGH	see Fig.4	1.2	–	–	–	ns
			2.7	3.0	–	–	ns
			3.0 to 3.6	3.0	1.5(2)	–	ns
t_{su}	set-up time nDn to nCP	see Fig.5	1.2	–	–	–	ns
			2.7	1.9	–	–	ns
			3.0 to 3.6	1.9	0.3(2)	–	ns
t_h	hold time nDn to nCP	see Fig.5	1.2	–	–	–	ns
			2.7	1.1	–	–	ns
			3.0 to 3.6	1.5	–0.3(2)	–	ns
$t_{sk(0)}$	skew		3.0 to 3.6	–	–	1.0	ns
f_{max}	maximum clock pulse frequency	see Fig.4	2.7	80	–	–	MHz
			3.0 to 3.6	100	150(2)	–	MHz

Notes

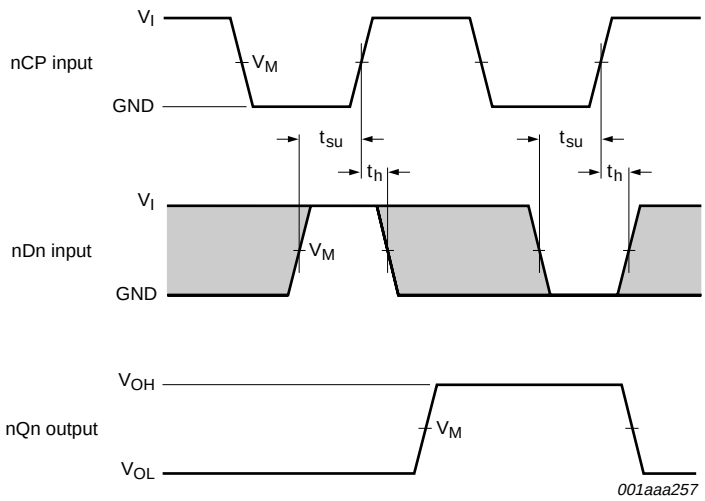
1. All typical values are measured at $T_{amb} = 25$ °C.
2. These typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS



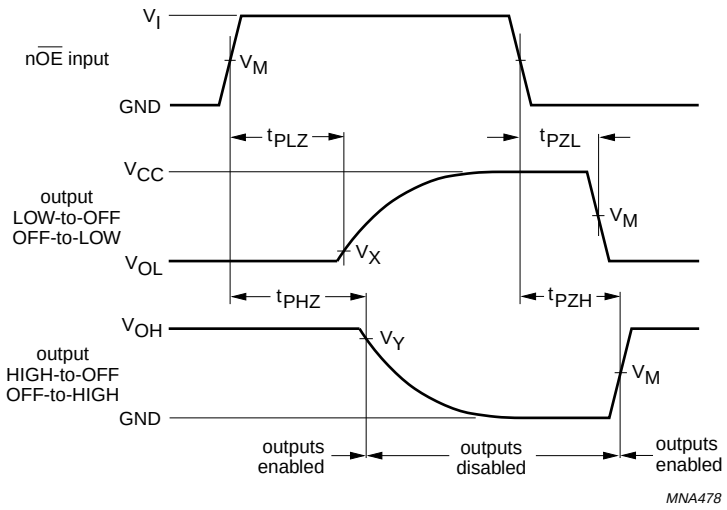
V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.4 Clock (nCP) to output (nQn) propagation delays, the clock pulse width and the maximum clock frequency.



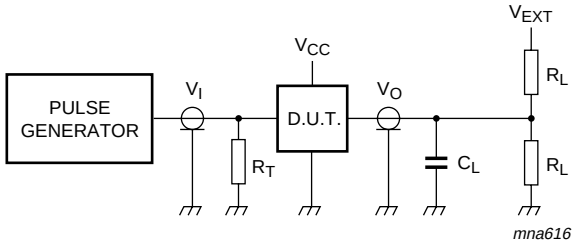
V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.5 Set-up and hold times for inputs (nDn) to inputs (nCP).



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V.
$V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V;
$V_X = V_{OL}$ + 0.1 V at V_{CC} < 2.7 V.
$V_Y = V_{OH}$ − 0.3 V at $V_{CC} \geq$ 2.7 V;
$V_Y = V_{OH}$ − 0.1 V at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.6 3-state output enable and disable times.



V_{CC}	V_I	C_L	R_L	V_{EXT}		
				t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
1.2 V	V_{CC}	50 pF	500 Ω(1)	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

Note

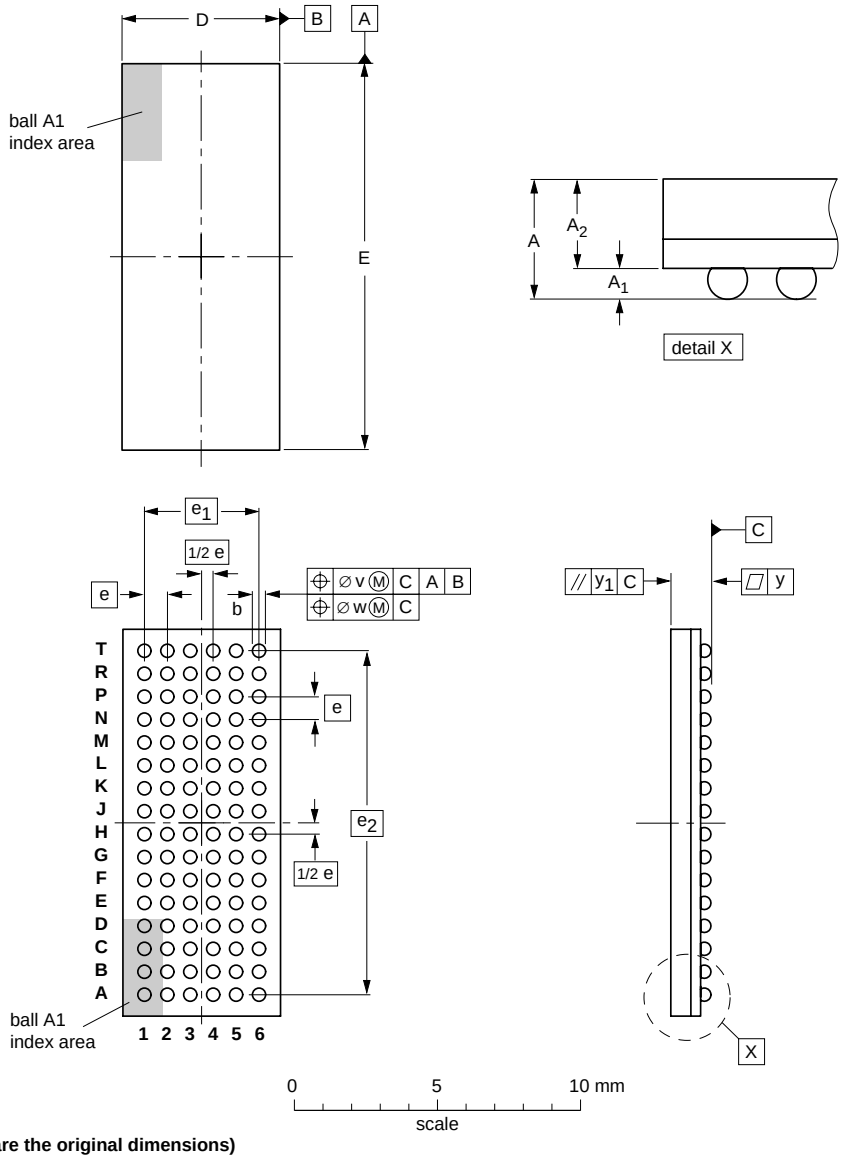
1. The circuit performs better when RL = 1000 Ω.

Definitions for test circuit:
R_L = Load resistor.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Load circuitry for switching times.

PACKAGE OUTLINE

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.5	0.41 0.31	1.2 0.9	0.51 0.41	5.6 5.4	13.6 13.4	0.8	4	12	0.15	0.1	0.1	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT536-1						~~00-03-04~~ 03-02-05

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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